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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,216	02/11/2004	Teruo Okada	040057	9967

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EXAMINER	
AMRANY, ADI	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 11/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,216	OKADA ET AL.	
	Examiner	Art Unit	
	Adi Amrany	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 13-18, 20-22 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tominaga (US 5,237,208) in view of Otani (US 7,045,915).

With respect to claim 28, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9), wherein;

at least two of the plurality of power source circuits are connected by a synchronous line (figure 2, item 20, and column 5, lines 22-26),

first and second power source circuits connected by the synchronous line comprise independent control circuits (figure 2, and column 5, lines 22-26),

the control circuits provided in the first and second power source circuits respectively comprise:

frequency synchronization means (figure 2, item 27, and column 5, lines 50-56, and column 7, lines 43-58) for controlling switching frequency of own circuit by using a synchronous signal outputting to the synchronous line;

abnormality signal detection means (column 8, lines 29-34) for detecting the abnormality signal outputted to the synchronous line and shutting down the own circuit;

a drive circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49) that generates a switching signal for controlling an output voltage; and

a voltage monitoring circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49)

Tominaga does not expressly disclose at least two power source circuits output mutually different output voltages.

Otani discloses a multiple output power source apparatus (figure 1; column 1, lines 65-67; column 3, lines 1-11) comprising a plurality of power source circuits (figure 1, items 11-1n) that output mutually different output voltages.

Tominaga and Otani are analogous art because they are from the same field of endeavor, namely parallel power systems. At the time of the invention by applicant it would have been obvious to a person of ordinary skill in the art to combine the power source apparatus disclosed in Tominaga with the multiple output voltage levels disclosed in Otani. The motivation for doing so would have been to supply a multiplicity of power supply voltages.

With respect to claim 13, Tominaga and Otani disclose the multiple output power source apparatus according to claim 28, and Tominaga further discloses;

the synchronous signal comprises a clock signal (column 5, lines 49-55) of a predetermined frequency,

the abnormality signal is generated by changing the clock signal (column 8, lines 5-34, namely lines 29-34),

the abnormality signal detection means detects change of the clock signal (column 5, lines 56-63).

With respect to claim 14, Tominaga further discloses the change of the clock signal is generated by the first power source circuit and/or second power source circuit (column 8, lines 5-34, namely lines 18-23).

With respect to claim 15, Tominaga further discloses the change of the clock signal is implemented by stopping the clock signal (column 6, line 62 to column 7, line 5), and the abnormality signal detection manes measures an interval during which the clock signal is stopped and shuts down the own circuit when it is detected that the stop state continues for a predetermined interval or longer (column 7, lines 23-29).

With respect to claim 16, Tominaga further discloses the change of the clock signal is implemented by changing a voltage level of the clock signal (column 8, lines 18-23) and the abnormality signal detection means measures the voltage level of the clock signal (column 8, lines 29-34) and shuts down (column 8, lines 32-34, release of failure signal "F") the own circuit when a predetermined voltage level is detected.

With respect to claim 17, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2,

and 3, and column 5, lines 4-9) equipped with independent output control circuits (figure 2, and column 5, lines 22-26), wherein the output control circuits comprise:

abnormality signal output means (figure 2, items 34, 38; column 6, lines 9-22 and 48-52);

means for controlling a drive circuit (figure 2, item 35; column 5, lines 46-49);

Tominaga does not expressly disclose at least two power source circuits output mutually different output voltages.

Otani discloses a multiple output power source apparatus (figure 1; column 1, lines 65-67; column 3, lines 1-11) comprising a plurality of power source circuits (figure 1, items 11-1n) that output mutually different output voltages.

With respect to claim 18, Tominaga further discloses an abnormality signal input means (figure 3, column 6, lines 14-22, and column 6, line 46 to column 7, line 5), and operation shutdown means (figure 3, and column 7, lines 6-29).

With respect to claim 20, Tominaga further discloses the operation of a power source circuit selected from the plurality of power source circuits equipped with the independent output control circuits is continued by the independent output control circuit even when the abnormality signal has been outputted from the other power source circuits (column 6, lines 56-61).

With respect to claim 21, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2,

and 3, and column 5, lines 4-9) equipped with independent output control circuits (figure 2, and column 5, lines 22-26), wherein the power source circuits comprise:

synchronous oscillation signal output means (column 7, lines 33-42);

a drive circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49) that generates a switching signal for controlling an output voltage; and

an output voltage monitoring circuit (figure 2, item 35);

means for controlling the drive circuit by an output of the output voltage monitoring circuit (figure 2, item 35).

Tominaga does not expressly disclose at least two power source circuits output mutually different output voltages. Otani discloses a multiple output power source apparatus (figure 1; column 1, lines 65-67; column 3, lines 1-11) comprising a plurality of power source circuits (figure 1, items 11-1n) that output mutually different output voltages.

With respect to claim 22, Tominaga further discloses a synchronous oscillation signal input means (figure 4, and column 7, lines 43-48), and control means (column 7, lines 49-58) for conducting synchronous control of a switching oscillation frequency.

With respect to claim 24, Tominaga further discloses the operation of a power source circuit selected from the plurality of power source circuits is continued by the output control circuit even when the abnormality signal has been outputted from the other power source circuits (column 6, line 46 to column 7, line 5, namely column 6, lines 56-61).

With respect to claim 25, Tominaga further discloses a control means for synchronously controlling a switching phase (column 7, lines 43-55) used for output control of the own circuit by a switching phase of the synchronous oscillation signal by the synchronous oscillation signal input means.

With respect to claim 26, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9), wherein;

at least two of the plurality of power source circuits are connected by a synchronous line (figure 2, item 20, and column 5, lines 22-26),

first and second power source circuits connected by the synchronous line comprise independent control circuits (figure 2, and column 5, lines 22-26), respectively,

the control circuit provided in the first power source circuit comprises:

synchronous signal output means (column 7, lines 33-42);

abnormality signal output means (figure 2, item 34, and column 6, lines 9-13);

a drive circuit (figure 2, item 35; figure 6, items 351-353; column 5, lines 46-49);

a voltage monitoring circuit (figure 2, item 35); and

means for controlling the switching signal generated from the drive circuit by an output of the voltage monitoring circuit (figure 2, item 35);

the control circuit provided in the second power source circuit comprises:

synchronous signal input means (column 7, lines 43-55);

abnormality signal input means (column 6, lines 14-23);

a drive circuit (figure 2, item 35);

a voltage monitoring circuit (figure 2, item 35); and

means for controlling the switching signal generated from the drive circuit by an output of the voltage monitoring circuit (figure 2, item 35);

Tominaga does not expressly disclose at least two power source circuits output mutually different output voltages. Otani discloses a multiple output power source apparatus (figure 1; column 1, lines 65-67; column 3, lines 1-11) comprising a plurality of power source circuits (figure 1, items 11-1n) that output mutually different output voltages.

With respect to claim 27, Tominaga further discloses

the control circuit provided in the first power source circuit further comprises abnormality signal input means (column 7, lines 1-5) for inputting the abnormality signal outputted to the synchronous line into the own circuit,

the control circuit provided in the second power source circuit further comprises abnormality signal output means (column 6, lines 46-68) for outputting the abnormality signal indicating the abnormality occurrence in the own circuit to the synchronous line, and

the first and second power source circuits shut down (column 7, lines 6-29) the own circuits when the abnormality signal has been inputted form the synchronous line.

3. Claims 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tominaga, in view of Otani, and in further view of Luo (US 2005/0073783).

Tominaga and Otani disclose the apparatus according to claims 18 and 22, as discussed above, but do not expressly disclose conducting input and output of the abnormality signal or the synchronous signal using a single terminal.

Luo discloses the abnormality signal output means and the abnormality input means conduct input and output of the abnormality signal by using a single terminal (figure 1, "comm line" 23 connects to each power source circuit at a single terminal, and paragraph 36), and further discloses the synchronous oscillation signal out means and the synchronous oscillation input means conduct input and output by using a single terminal (figure 1, "sync" line connects to each power source circuit at a single terminal, and paragraph 35).

Tominaga, Otani and Luo are analogous art because they are from the same field of endeavor, namely parallel power systems. At the time of the invention by applicant it would have been obvious to a person of ordinary skill in the art to combine the power source apparatus disclosed in Tominaga and Otani with the single terminal configuration disclosed in Luo. The motivation for doing so would have been to reduce wiring required to transmit between modules.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adi Amrany whose telephone number is (571) 272-0415. The examiner can normally be reached on weekdays, from 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA

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